'003 patent"); Claim 12 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '693 patent in view of the '003 patent, further in view of U.S. Patent No. 4,467,452 to Saito et al. (hereinafter "the '452 patent"); and Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '693 patent in view of the '003 patent, further in view of U.S. Patent No. 5,731,130 to Tseng (hereinafter "the '130 patent").

Amended Claim 1 is directed to a nonvolatile semiconductor memory device including (1) a semiconductor substrate, (2) an element isolation region formed in the substrate, (3) a first transistor formed in a peripheral circuit portion of the substrate, (4) a second transistor formed in a memory cell portion of the substrate, (5) a contact, and (6) a first insulating film, not formed of silicon oxide, covering the second transistor. Claim 1 has been amended, without adding new matter, to recite the element isolation region; that the first transistor includes source and drain diffusion layers and a gate electrode; that the second transistor includes source and drain diffusion layers and a gate electrode having a gate length shorter than the gate electrode of the first transistor; and that the first insulating film is different from silicon oxide, does not cover the first transistor, and is an etching stopper for the contact to the element isolation region.

The '693 patent, cited in the rejection of Claim 1, is directed to a semiconductor memory device having a MOS transistor and a floating gate type MOS transistor. The Office Action indicates that the '693 patent discloses an insulating film 158 covering a second transistor. Regarding this insulating film, the '693 patent discloses:

> In the high-temperature heat-treatment step, the surfaces of the semiconductor substrate 128, floating gate 122, control gate 124 and gate electrodes 138c and 138d are *thermally oxidized* to form a third oxide film 158.[3]

[3] '693 patent, column 11, lines 19-23 (emphasis added).

In contrast, the insulating film of Claim 1 is *not* formed of silicon oxide, but of a material that is more effective than silicon oxide at preventing the penetration of an oxidizing agent (such as silicon nitride), as recited in amended Claim 1. Thus, since the '693 patent does not disclose the claimed insulating film, Applicants respectfully traverse the rejection of Claim 1 (and dependent Claims 2, 3, and 5) as being anticipated by the '693 patent.

Regarding the rejection of Claims 1-3 and 5 under 35 U.S.C. §103(a) as being unpatentable over the '693 patent, Applicants submit that the Office Action has failed to indicate which elements recited in Claim 1 are not disclosed by the '693 patent. Further, the Office Action has not provided any evidence that one of ordinary skill in the art would have been motivated to modify the '693 patent to obtain the claimed semiconductor memory device, or that such a modification would have been obvious. Thus, Applicants respectfully submit that a *prima facie* case of obviousness has not been established. Accordingly, the rejection should be withdrawn.

Amended Claim 11 is directed to a nonvolatile semiconductor memory device including a semiconductor substrate, a plurality of memory cell transistors, a plurality of peripheral transistors, and an insulating film. Claim 11 has been amended to include the plurality of peripheral transistors and add the limitations that (1) the insulating film is comprised primarily of silicon and nitrogen, (2) the surface of the insulating film is oxidized, and (3) the insulating film covers a side and a top of each memory cell transistor and each peripheral transistor.

In regard to the rejection of Claims 4, 11, and 14 as unpatentable over the '693 and '003 patents, the Office Action states that the '693 patent teaches everything in the claims with the exception of the insulating film, and relies on the '003 patent to remedy the deficiency. The '003 patent discloses that "the gate electrode 6 is covered with an

intermediate insulating layer 7 of phosphorus-doped silicon dioxide or phosphosilicate glass which extends over the source region 3 and the drain region 4..." and that "[t]he entire surface is covered with a passivation layer 12 of silicon nitride...."[4] However, the '003 patent fails to disclose an insulating film comprised primarily of silicon and nitrogen in which the surface of the insulating film is oxidized, as recited in amended Claim 11.

Thus, no matter how the teachings of the '693 and '003 patents are combined, the combination does not teach or suggest the claimed insulating film. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claim 11 (and dependent Claim 14) should be withdrawn. In addition, the rejection of Claim 4 is rendered moot since Claim 4 has been canceled by the present amendment.

In regard to the rejection of Claim 12, which depends from Claim 11, as being unpatentable over the '693, '003, and '452 patents, the Office Action relies on the '452 patent to disclose the thickness of the insulating film. However, Applicants respectfully submit that the '452 patent does not cure the deficiencies of the '693 and '003 patents with regard to the claimed insulating film, namely that the surface of the insulating film is oxidized. Thus, Applicants respectfully traverse the rejection of Claim 12 as being unpatentable over the 693, '003, and '452 patents.

In regard to the rejection of Claim 13, which depends from Claim 11, as being unpatentable over the '693, '003, and '130 patents, the Office Action relies on the '130 patent to disclose the thickness of an oxidized region of the insulating film. The '130 patent discloses a silicon nitride interelectrode dielectric film 40 on the surface of the capacitor bottom electrodes. However, Applicants respectfully submit that the '130 patent does not

---

[4]Id., column 3, lines 27-30 and 37-38.

cure the deficiencies of the '693 and '003 patents with regard to the claimed insulating film, as discussed above. Thus, Applicants respectfully traverse the rejection of Claim 13 as being unpatentable over the 693, '003, and '130 patents.

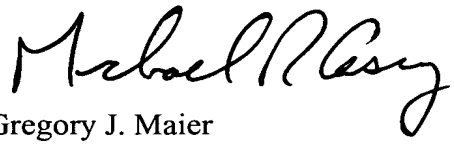
The present response also sets forth new Claims 19-25 for examination. Applicants respectfully submit that new Claims 19 and 20, which depend from Claim 11, are allowable for the reasons set forth above for the patentability of Claim 11. Independent Claim 21 is directed to a nonvolatile semiconductor memory device including a semiconductor substrate; an element isolation region; a plurality of erasable and programmable memory cell transistors; a plurality of peripheral transistors; a contact; and an etching stopper insulating film having an oxidized surface. Since the claimed etching stopper insulating film is analogous to the insulating film recited in Claim 11, Applicants submit that Claim 21 (and dependent Claims 22-25) are patentable over the cited references.

Thus, it is respectfully submitted that independent Claim 1 (and its dependent Claims 2, 3, and 5), independent Claim 11 (and its dependent Claims 12-14, 19 and 20), and independent Claim 21 (and its dependent Claims 22-25) patentably define over the '693, '003, '452, and '130 patents.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Registration No. 25,599
Michael R. Casey, Ph.D.
Registration No. 40,294
Attorneys of Record

22850

Tel. No. (703) 413-3000
Fax No. (703) 413-2220
GJM:MRC:KMB:fbl
I:\atty\kmb\0039\00397692.am.wpd

Marked-Up Copy
Serial No: 09/556,777
Amendment Filed on: _____

IN THE SPECIFICATION

Please amend the paragraph beginning on page 5, line 17 as follows:

[A first object of this invention is to provide a nonvolatile semiconductor memory device in which the annealing condition for diffusion of impurity and post oxidation amount can be controlled according to the gate lengths of transistors to attain the high performance of the device and a method for manufacturing the same] A nonvolatile semiconductor memory device according to an aspect of the present invention comprises: a semiconductor substrate; and element isolation region formed in the semiconductor substrate, the element isolation region isolating a plurality of element regions in the semiconductor substrate; a first transistor formed in a peripheral circuit portion of the semiconductor substrate, the first transistor including source and drain diffusion layers formed in one of the plurality of element regions and a gate electrode having a first gate length, a second transistor formed in a memory cell portion of the semiconductor substrate, the second transistor including source and drain diffusion layers formed in another of the plurality of element regions and a gate electrode having a second gate length shorter than the first gate length; a contact connected to the one of the source and drain diffusion layers; and a first insulating film different from a silicon oxide covering the second transistor and not covering the first transistor, the first insulating film being an etching stopper for the contact to the element isolation region and having a property which makes it difficult for an oxidizing agent to pass therethrough

compared with the silicon oxide.

Paragraph beginning on page 5, line 24. (Deleted)

Paragraph beginning on page 6, line 2. (Deleted)

Paragraph beginning on page 6, line 16. (Deleted)

Paragraph beginning on page 6, line 26. (Deleted)

Paragraph beginning on page 7, line 8. (Deleted)

Paragraph beginning on page 7, line 15. (Deleted)

Paragraph beginning on page 8, line 1. (Deleted)

Paragraph beginning on page 8, line 8. (Deleted)

Paragraph beginning on page 8, line 16. (Deleted)

IN THE CLAIMS

Please cancel Claim 4 without prejudice.

Please amend the Claims 1-3 and 11-14 as follows:

1. (Amended) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

an element isolation region formed in the semiconductor substrate, the element isolation region isolating a plurality of element regions in the semiconductor substrate;

a first transistor formed in a peripheral circuit portion of the semiconductor substrate, [a gate electrode of the first transistor having a first gate length] the first transistor including source and drain diffusion layers formed in one of the plurality of element regions and a gate electrode having a first gate length;

a second transistor formed in a memory cell portion of the semiconductor substrate, [a gate electrode of the second transistor having a second gate length shorter than the first gate

length] the second transistor including source and drain diffusion layers formed in another of the plurality of element regions and a gate electrode having a second gate length shorter than the first gate length; [and]

a contact connected to one of the source and drain diffusion layers; and

a first insulating film different from a silicon oxide [formed above at least the memory cell portion, the first insulating film] covering the second transistor and not covering the first transistor, the first insulating film being an etching stopper for the contact to the element isolation region and having a property which makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide.

2. (Amended) The nonvolatile semiconductor memory device according to claim 1, wherein the gate electrode of the second transistor has a stacked gate structure which includes a floating gate formed on a gate insulating film, an inter-gate insulating film formed on the floating gate and a control gate including a metal or a metal compound containing silicon formed on the inter gate insulating film.

3. (Amended) The nonvolatile semiconductor memory device according to claim 1, further comprising:

a second insulating film which is different from the first insulating film and formed between at least the gate electrode of the second transistor[s] and the first insulating film.

11. (Amended) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a [transistor formed in a memory cell portion of the semiconductor substrate] plurality

of erasable and programmable memory cell transistors; [and]

a plurality of peripheral transistors comprising peripheral circuits;

[a silicon nitride film whose surface is oxidized, the silicon nitride film covers the transistor] an insulating film covering a side and a top of both the plurality of erasable and programmable memory cell transistors and the plurality of peripheral transistors, the insulating film comprised primarily of silicon and nitrogen, and a surface of the insulating film being oxidized.

12. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the [silicon nitride] insulating film has a thickness of at most 50 nm.

13. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the thickness of [an oxide film on the surface of the silicon nitride film] an oxidized region of the insulating film is not smaller than 1 nm and not larger than 10 nm.

14. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the concentration of hydrogen in the [silicon nitride film] insulating film is not larger than 3×10^{21} atom/cm^3.

IN THE ABSTRACT

Please amend page 38, lines 2-13 as follows:

[A nonvolatile semiconductor memory device having a memory cell portion and peripheral circuit portion is disclosed. The nonvolatile semiconductor memory device has peripheral transistors formed in the peripheral circuit portion of a silicon substrate and cell

transistors formed in the memory cell portion of the silicon substrate. The gate length of the cell transistor is shorter than the gate length of the peripheral transistor. Further, the nonvolatile semiconductor memory device has a silicon nitride film selectively formed on the memory cell portion. The silicon nitride film covers the cell transistors] A first transistor formed in a peripheral circuit portion of a semiconductor substrate. The first transistor includes source and drain diffusion layers formed in one element region. A second transistor formed in a memory cell portion of the semiconductor substrate. The second transistor includes source and drain diffusion layers in another element region. A contact connected to the one of the source and drain diffusion layers. A first insulating film different from a silicon oxide covers the second transistor. The first insulating film is an etching stopper for the contact to the element isolation region and has a property which makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide.